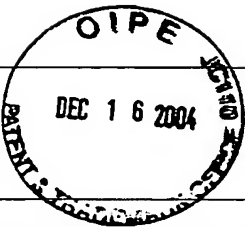


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U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

**REQUEST FOR CERTIFICATE OF  
CORRECTION PURSUANT TO  
37 C.F.R. § 1.322**

Docket Number:  
**10191/2235**

Conf. No.:  
**4101**

Application Number  
**10/049,474**

Filing Date  
**July 18, 2002**

Examiner  
**TRAN, Minh Loan**

Art Unit  
**2826**

Patent Number  
**6,716,714**

Issue Date  
**April 6, 2004**

**Certificate**

Invention Title  
**SEMICONDUCTOR DIODE AND METHOD  
FOR PRODUCING THE SAME**

Inventor(s)  
**Herbert GOEBEL et al.**

**DEC 22 2004**

**of Correction**

Address to:

Commissioner For Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

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22313-1450  
on

Date:

Signature:

12/13/04  
*[Signature]*  
S. Grustini

We have compared the above patent with the application as filed and have found errors in the printing of the patent. We respectfully request that the enclosed Certificate of Correction on Form PTO-1050 be issued correcting the mistakes set forth therein under authority of 35 U.S.C. §254. The exact column and line number where the errors occur in the patent are listed on the enclosed certificate.

The errors that appear in this patent are Patent Office errors and no fee is believed required. However, if necessary, please charge any fee or credit any overpayment to Deposit Account No. 11-0600.

Dated:

12/13/04

By:

*[Signature]*  
Richard L. Mayer, Reg. No. 22,490

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DEC 27 2004



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DEC 27 2004

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

**PATENT No. :** 6,716,714  
**DATED :** April 6, 2004  
**INVENTOR(S):** Herbert GOEBEL et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the face of the patent, # (57) Abstract, line 8, change "voltage of diode." to -- voltage of the diode--

Column 1, line 33, change "the silicon" to --the silicon chip, the allowable current load to be increased and the thermal loading of the silicon chip to be reduced in a manner that can be realized relatively simply. In so doing, a reduction in the forward voltage is simultaneously achieved. The effect of additional saw grooves is particularly advantageous, because later, when the socket and lead wire are soldered to the diode chip, the grooves lead to a better, bubble-free soldering procedure (capillary effect), and the grooves filled with solder result in additional, more effective cooling of the chip, which extends into the depth of the silicon body and therefore thermally couples the chip to the heat sink in a more effective manner.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1a shows a cross-sectional side view of a diode in accordance with the present invention.

Fig. 1b shows a plan view of the diode shown in Fig. 1a.

Fig. 2 shows a semiconductor wafer used as the starting material in a method for producing the semiconductor arrangement in accordance with the present invention.

Fig. 3 shows the semiconductor wafer in a further method step for producing the semiconductor arrangement in accordance with the present invention.

Fig. 4 shows the semiconductor wafer in yet another method step for producing the semiconductor arrangement in accordance with the present invention.--

Column 2, line 43, change "neutral is filing" to --neutral filing--

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Kenyon & Kenyon  
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New York, NY 10004

**Patent No. 6,716,714 B1**

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